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## PATENT ABSTRACTS OF JAPAN

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H03L 7/081(21) Application number: 10205309  
(22) Date of filing: 21.07.1998(71) Applicant: NEC CORP  
(72) Inventor: MIZUNO MASA HARU(54) LOW SKEW CLOCK TREE CIRCUIT USING  
VARIABLE THRESHOLD VOLTAGE  
TRANSISTOR

(57) Abstract:

PROBLEM TO BE SOLVED: To provide a clock tree circuit capable of controlling clock skew of a clock tree circuit, reduced in power consumption and low in clock skew.

SOLUTION: This clock tree circuit uses a transistor having a threshold voltage variable well structure for a clock element. Here, it has phase comparator circuits 31 to 33 which perform comparison observation of skew values among respective elements 21 to 24 and output differential voltage and charge pump circuits 41 to 43 which make the differential voltage of the circuits 31 to 33 inputs and supply them as well potential to each well terminal of the elements 21 to

24, controls the switching speed of a clock tree circuit - by adjusting the threshold voltage of each element 21 to 24 and reduces clock skew.

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